Amendments to the Claims

1. (CURRENTLY AMENDED) A circuit comprising: a pulse generator ~~(140)~~ capable of generating a masking pulse timed and of sufficient duration to block at a device ~~(100)~~ a reflection signal within a received signal from a transmission line; and logic ~~(130)~~ for combining the masking pulse with the received signal, wherein the reflection signal is substantially blocked by the masking pulse at a blocking filter ~~(120)~~.

2. (CURRENTLY AMENDED) The circuit of claim 1, wherein the pulse generator ~~(140)~~ comprises at least one memory element ~~(142)~~ and a delay circuit ~~(144)~~, wherein an inverted output of the logic ~~(130)~~ drives a set input of the at least one memory element ~~(142)~~, an output of the delay circuit ~~(144)~~ drives a reset input of the at least one memory element ~~(142)~~, and an output of the at least one memory element ~~(142)~~ is inverted and provided as input to the logic ~~(130)~~ as the masking pulse.

3. (CURRENTLY AMENDED) The circuit of claim 2, wherein the pulse generator ~~(140)~~ further comprises delay logic for lengthening the masking pulse, said delay logic being connected between the output of the delay circuit and the reset input of the at least one memory element, wherein the delay logic also receives as input the received signal from the transmission line.

4. (ORIGINAL) The circuit of claim 2, further comprising an extender circuit connected between the pulse generator and the logic for combining the masking pulse, wherein the extender circuit extends the duration of the masking pulse until the received signal falls a second time or rises a second time depending upon whether the reflection signal is on a falling edge or a rising edge, respectively, of a state change in the received signal.

5. (CURRENTLY AMENDED) The circuit of claim 4, wherein the extender circuit comprises at least one latch ~~(170)~~, with a set input of the at least one latch ~~(170)~~ receiving output from the at least one memory element ~~(142)~~ of the pulse generator ~~(140)~~, a reset input of the at least one latch ~~(170)~~ comprising the received signal inverted, and an output of the at least one latch ~~(170)~~ being forwarded for

combining with the output of the pulse generator ~~(140)~~ before being forwarded to the logic ~~(130)~~ for combining of the masking pulse and the received signal.

6. (ORIGINAL) The circuit of claim 4, wherein the extender circuit comprises multiple latches and multiple NOR gates for extending the masking pulse when triggered on either a falling edge or a rising edge of the received signal, and wherein the pulse generator includes multiple memory elements for generating the masking pulse on both the falling edge and rising edge of the received signal.

7. (ORIGINAL) The circuit of claim 1, wherein the transmission line has mismatched impedance termination at an output end thereof.

8. (CURRENTLY AMENDED) The circuit of claim 1, wherein the device ~~(100)~~ is a receiver device which is connected closer to an input end of the transmission line than an output end of the transmission line.

9. (CURRENTLY AMENDED) The circuit of claim 1, wherein the blocking filter comprises a digital filter circuit ~~(120)~~ disposed at an input of the device ~~(100)~~.

10. (CURRENTLY AMENDED) A network comprising: a bus system having a transmission line, wherein a reflection signal arises with transmission of a signal across the transmission line; a device ~~(100)~~ connected to the transmission line for receiving the signal, the device including a blocking filter ~~(120)~~ comprising: a pulse generator ~~(140)~~ for generating a masking pulse timed and of sufficient duration to block the reflection signal, and logic ~~(130)~~ for combining the masking pulse with the signal received from the transmission line, wherein the reflection signal is blocked by the masking pulse.

11. (CURRENTLY AMENDED) The network of claim 10, wherein the device ~~(100)~~ is connected closer to an input end of the transmission line than an output end of the transmission line, and wherein the blocking filter ~~(120)~~ comprises a digital filter circuit disposed at an input of the device.

12. (CURRENTLY AMENDED) The network of claim 10, wherein the pulse generator ~~(140)~~ of the blocking filter ~~(120)~~ further comprises at least one memory element ~~(142)~~ and a delay circuit ~~(144)~~, wherein an inverted output of the logic drives a set input of the at least one memory element ~~(142)~~, an output of the delay circuit ~~(144)~~ drives a reset input of the least one memory element ~~(142)~~, and an

output of the least one memory element ~~(142)~~ is inverted and provided as input to the logic ~~(130)~~ as the masking pulse.

13. (CURRENTLY AMENDED) The network of claim 12, wherein the pulse generator ~~(140)~~ further comprises delay logic for lengthening the masking pulse, said delay logic being connected between the output of the delay circuit ~~(144)~~ and the reset input of the at least one memory element ~~(142)~~, wherein the delay logic also receives as input the received signal from the transmission line.

14. (ORIGINAL) The network of claim 12, further comprising an extender circuit connected between the pulse generator and the logic for combining the masking pulse, wherein the extender circuit extends the duration of the masking pulse until the received signal falls a second time or rises a second time depending upon whether the reflection signal is on a falling edge or a rising edge, respectively, of a state change in the received signal.

15. (ORIGINAL) The network of claim 14, wherein the extender circuit comprises at least one latch, with a set input of the at least one latch receiving output from the at least one memory element of the pulse generator, a reset input of the at least one latch comprising the received signal inverted, and an output of the at least one latch being forwarded for combining with the output of the pulse generator before being forwarded to the logic for combining of the masking pulse and the received signal.

16. (ORIGINAL) The network of claim 14, wherein the extender circuit comprises multiple latches and multiple NOR gates for extending the masking pulse when triggered on either a falling edge or a rising edge of the received signal, and wherein the pulse generator includes multiple memory elements for generating the masking pulse on both the falling edge and the rising edge of the received signal.

17. (ORIGINAL) A method of comprising: generating a masking pulse timed and of sufficient duration to substantially block at a device connected to a transmission line a reflection signal within a received signal from the transmission line; and combining the masking pulse with the received signal, wherein the reflection signal is substantially blocked by the masking pulse.

18. (ORIGINAL) The method of claim 17, further comprising lengthening the masking pulse prior to combining thereof with the received signal to insure that

the masking pulse completely blocks the reflection signal, said lengthening being accomplished in part by using the received signal.

19. (ORIGINAL) The method of claim 17, further comprising generating the masking pulse on either a falling edge or a rising edge of a state change in the received signal, wherein a reflection signal on either the falling edge or the rising edge is substantially blocked by the masking pulse.

20. (ORIGINAL) The method of claim 17, further comprising implementing the method within a digital filter circuit disposed at an input of the device connected to the transmission line.

21. (ORIGINAL) A circuit comprising: means for generating a masking pulse timed and of sufficient duration to substantially block at a device connected to a transmission line a reflection signal within a received signal from the transmission line; and means for combining the masking pulse with the received signal, wherein the reflection signal is substantially blocked by the masking pulse.